REMARKS

Claims 1-3 and 5-14 are pending in this application. By this Amendment, claims 1, 2, 5, 8, 10 and 14 are amended. These amendments are supported by Applicant's specification at least at, Figures 3-7 and page 13, lines 21-27. The drawings are amended. Claim 15 is cancelled without prejudice to or disclaimer of the subject matter that this claim recites. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

Objection to the Drawings

The drawings were objected to in the Office Action. In the Office Action it is asserted that Figure 8 allegedly shows prior art. Figure 8 is amended to obviate this objection. Withdrawal of the objection to the drawings is respectfully requested.

Rejection under 35 U.S.C. §112, second paragraph

Claims 1-3 and 5-15 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. Claims 1, 10 and 14 are amended and claim 15 is cancelled to obviate this rejection. In the Office Action it is asserted that it is unclear which bus is referenced in claim 2. The context bus has antecedent basis at line 15 in claim 1. Claim 2 recites wherein the context switching bus has a bus width greater than a bit width of the register file. Thus, claim 2 does not refer to any other bus, only a bus width (the bus being width the number of parallel connections that form the bus). Therefore, claim 2 is not indefinite.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-3 and 5-15 under 35 U.S.C. §112, second paragraph, are respectfully requested.

Rejection under 35 U.S.C. §101

Claims 14 and 15 were rejected under 35 U.S.C. §101 as allegedly being drawn to non-statutory subject matter. Claim 14 is amended and claim 15 is canceled to obviate this rejection. In particular, claim 14 is amended to recite a computer comprising a context switching program to obviate this rejection.

Accordingly, reconsideration and withdrawal of the rejection of claims 14 and 15 under 35 U.S.C. §101 are respectfully requested.

Rejections under 35 U.S.C. §103

Claims 1, 3 and 5-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,351,808 to Joy in view of Parallel replacement mechanism for multithread, 1997, pages 338-343 by Cui et al. (hereinafter "Cui"). This rejection is respectfully traversed.

It was conceded in the Office Action that Joy does not teach wherein the thread control unit receives a context switch instruction for executing a save operation and a restore operation concurrently and when a context switch which executes both a context save operation and a context restore operation in parallel occurs; sends the register identifier to the register file concurrently; the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context to the context-switching write port through the restore bus, in the register corresponding to the register identifier; concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and the context switching unit switches contexts by executing an operation for restoring a context from the context to the register file and an operation for saving a context from the register file to the context concurrently. It was asserted in the Office Action that Cui remedies these shortfalls of Joy. The analysis of the Office Action fails for the following reasons.

Claims 1, 10 and 14 recite, among other features, the context cache being not connected to a memory through a bus, which connects the memory, an instruction cache and a data cache to each other, and being independent from a memory system including the memory.

Joy teaches at, e.g., Figure 12, a processor 1200 and processor architecture that are for implementing various multithreading techniques and system implementations that improve multithreading performance and functionality. The processor 1200 also includes a set of integer registers 1248, floating-point registers 1250 and a data cache 1256. The integer registers 1248, floating-point registers 1250 and the data cache 1256 are connected by a 128 bit wide bus that also connects to cache control system interface 1222 and instruction cache 1212 via predecode unit 1224. It is asserted in the Office Action that data cache 1256 of Joy corresponds to the context cache. As noted above, data cache 1256 is connected by a 128 bit wide bus that also connects to cache control system interface 1222 and instruction cache 1212 via predecode unit 1224. Thus, the data cache 1256 of Joy cannot reasonably be considered to have suggested a context cache as recited in claims 1, 10 and 14 because the data cache 1256 of Joy is connected to control system interface 1222 and instruction cache 1212 but the context cache is not connected to a memory through a bus, which connects the memory, an instruction cache and a data cache to each other, and being independent from a memory system including the memory, as recited in claim 1, 10 and 14.

Cui, as applied to claims 1, 10 and 14, does not remedy these shortfalls of Joy because Cui teaches, at, e.g. Figure 3_0 and 3_1 that the Cache and contexts CT1-CTn are connected to the Main Memory.

For at least the foregoing reasons, the combination of Joy with Cui cannot reasonably be considered to have suggested the combinations of all of the features recited in claims 1, 10 and 14. Further, the combination of Joy with Cui cannot reasonably be considered to have suggested the combinations of all of the features recited in claims 3, 5-9 and 11-13 for at least the dependence of these claims on allowable base claims, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejection of claims 1, 3 and 5-15 under 35 U.S.C. 103(a) as being unpatentable over Joy in view of Cui are respectfully requested.

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Joy in view of Cui further in view of U.S. Patent No. 6,526,491 to Suzuoki et al. (hereinafter "Suzuoki"). This rejection is respectfully traversed.

It was conceded in the Office Action that Joy and Cui do not teach wherein the context switching bus has a bus width greater than the bit width of the register file. It was asserted in the Office Action that Suzuoki remedies these shortfalls of Joy and Cui. As argued above, Joy and Cui cannot reasonably be considered to have suggested the combination of all of the features recited in claim 1. Suzuoki, as applied to claim 1, does not remedy the above-discussed shortfalls of Joy. Therefore, the combination of Joy with Cui and Suzuoki cannot reasonably be considered to have suggested the combination of all of the features recited in claim 2 for at least the dependence of this claim on an allowable base claim, as well as for the separately patentable subject matter that this claim recites.

Accordingly, reconsideration and withdrawal of the rejection of claim 2 under 35 U.S.C. 103(a) as being unpatentable over Joy in view of Cui further in view of Suzuoki are respectfully requested.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

Early issuance of a Notice of Allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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